

METHOD AND SYSTEM FOR FAST ETHERNET SERIAL PORT MULTIPLEXING TO REDUCE I/O PIN COUNT

Abstract of the Disclosure

A system and method of reducing the input and output pins used to interface a fast serial
5 port Ethernet processing system using multiplexing. Using the system of the present invention,
four pins can allow a plurality of Ethernet communication paths to be connected to a single
processor on a substrate. These four connections include a clocking input as well as a strobe
signal which coordinates the multiplexing and identifies the time period for a predetermined
source. The physical layer and the processor are each provided with a multiplexor which is
10 controlled by the strobe to select the network to be coupled at any given time. The multiplexor
includes a counter which is incremented by the clocking input and reset by the strobe signal.